

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An apparatus, comprising:
an input to receive a non-rate verified align detect signal over a serial interconnect;
a rate verification unit to determine whether ~~an appropriate number of incoming align~~
primitives are received at a target clock rate during a predetermined number of clock periods, the
rate verification unit including a shift register that is clocked at the target clock rate, the shift
register having a first flip flop to receive a non-rate verified align detect signal and to output a
first Last Align Detect signal; and
an output to deliver a rate-verified align detect signal to a core logic of the apparatus.
2. (Cancelled)
3. (Currently Amended) The apparatus of claim 1~~claim 2~~, the rate verification unit further including a checking logic unit.
4. (Original) The apparatus of claim 3, the rate verification unit further including a state machine.
5. (Cancelled)
6. (Currently Amended) The apparatus of claim 1~~claim 5~~, the shift register further including a second, a third, and a fourth flip-flop, the second flip-flop to receive the first Last Align Detect signal and to output a second Last Align Detect signal, the third flip-flop to receive the second Last Align Detect signal and to output a third Last Align Detect signal, and the fourth flip-flop to receive the third Last Align Detect signal and to output a fourth Last Align Detect signal.
7. (Currently Amended) The apparatus of claim 6, the rate verification unit further including a checking logic unit, the checking logic unit to receive the first, second, third, and

fourth Last Align Detect signals from the shift register, the checking logic unit to assert a nonaligndetected signal if each of the values of the first, second, third, and fourth Last Align Detect signals are zero.

8. (Currently Amended) The apparatus of claim 7, the checking logic unit further to assert the nonaligndetected signal if more than one K28.5 characters are sampled in a 4-byte sequence.

9. (Currently Amended) The apparatus of claim 7, the rate verification unit further including a state machine, the state machine to count up to n align detects, the count to increase each time the non-rate verified align detect signal is asserted and the count to reset each time the nonaligndetected signal is asserted.

10. (Original) The apparatus of claim 9, the state machine to cause the rate-verified align detect signal to be asserted.

11. (Original) The apparatus of claim 10, the state machine to keep the rate-verified align detect signal asserted until an acknowledge signal is received.

12. (Currently Amended) A system, comprising:
a serial interconnect host controller implemented according to a Serial ATA specification, including
a data recovery circuit to receive incoming serial input stream over a serial interconnect and to output a non-rate verified align detect signal; and
a rate verification unit to determine whether an appropriate number of incoming align primitives are received at a target clock rate during a predetermined number of clock periods, and to deliver a rate-verified align detect signal to a core logic of the serial interconnect host controller, the rate verification unit including a shift register that is clocked at the target clock rate, the shift register having a first flip flop to receive a non-rate verified align detect signal and to output a first Last Align Detect signal; and
a system component coupled to the serial interconnect host controller via the serial interconnect.

13. (Cancelled)
14. (Currently Amended) The system of ~~claim 12~~claim 13, wherein the system component is a mass storage device.
15. (Cancelled)
16. (Currently Amended) The system of ~~claim 12~~claim 15, the rate verification unit further including a checking logic unit.
17. (Original) The system of claim 16, the rate verification unit further including a state machine.
18. (Currently Amended) A rate verifying method, comprising:
receiving a serial input stream over a serial interconnect;
detecting an align sequence in the serial input stream;
determining at a rate verification unit whether ~~an appropriate number of incoming align~~ primitives are received at a target clock rate during a predetermined number of clock periods, the rate verification unit including a shift register that is clocked at the target clock rate, the shift register having a first flip flop to receive a non-rate verified align detect signal and to output a first Last Align detect signal; and
generating a rate-verified align detect signal.
19. (Currently Amended) The method of claim 18, wherein determining whether ~~an appropriate number of incoming align~~ primitives are received at a target clock rate during a predetermined number of clock periods includes using clock periods that conform to [[a]]the target clock rate.
20. (Cancelled)

21. (New) The method of claim 1, wherein an align primitive is received as every fourth non-rate verified align detect signal.
22. (New) The system of claim 12, wherein an align primitive is received as every fourth non-rate verified align detect signal.
23. (New) The method of claim 18, wherein an align primitive is received as every fourth non-rate verified align detect signal.
24. (New) The apparatus of claim 1, wherein the rate verification unit determines whether the incoming align primitives are received at the target clock rate or some other rate.
25. (New) The system of claim 12, wherein the rate verification unit determines whether the incoming align primitives are received at the target clock rate or some other rate.
26. (New) The method of claim 18, wherein the rate verification unit determines whether the incoming align primitives are received at the target clock rate or some other rate.
27. (New) The apparatus of claim 1, wherein the rate verification unit includes a detector to detect that the incoming align primitives are received prior to and in addition to determining whether the incoming align primitives are received at a target clock rate.
28. (New) The system of claim 12, wherein the rate verification unit includes a detector to detect that the incoming align primitives are received prior to and in addition to determining whether the incoming align primitives are received at a target clock rate.
29. (New) The method of claim 18, wherein detecting the align sequence occurs prior to and in addition to determining whether the incoming align primitives are received at a target clock rate.